Electronic Version
Stylesheet Version v1.1.1

METHOD FOR IMPROVING PROCESSING EFFICIENCY OF PIPELINE ARCHITECTURE

Abstract

A method for improved processing efficiency of pipeline architecture with a processor. The processor has a first functional unit;a second functional unit; and a control unit electrically connected to the first and the second functional units for generating a plurality of control signals to control the first and the second functional units. The method includes following steps:(a) executing a first calculation task with the first functional unit or the second functional unit; (b) determining an executing time period of a second calculation task with the control unit according to the functional unit executing the first calculation task, an executing time period of the first calculation task, and whether the second calculation task depends upon a result of the first calculation task; and (c) executing the second calculation task with the first functional unit according to the executing time period of the second calculation task determined in step (b).